

REMARKS

Favorable reconsideration of this application as amended is respectfully requested.

The objection to the drawings has been overcome by labeling Figs. 34-37 as Prior Art and by extending the lead line from reference character 1 in Fig. 34.

The title of the invention has been amended, as well as the first paragraph of the specification thereafter.

Claim 31 has been amended to clarify an important distinction between the invention and Toyoshima, relied upon in the rejection under 35 U.S.C. § 102(b). The preamble of Claim 32 has been amended to conform with the preamble of Claim 31. New Claims 33-36 have been added.

Claim 31 now recites a groove that is formed in the insulating film so as to expose the main surface of the wiring substrate between the plurality of electrodes and the semiconductor chip. New independent Claim 36 contains the same recitation.

When a covering operation is performed, as recited in Claims 31 and 36, voids tend to be formed around a peripheral edge portion of the semiconductor chip. To solve this problem, large quantities of the pasty adhesive are applied to the insulating film before mounting of the semiconductor chip on the insulating film. Therefore, the pasty adhesive tends to flow to the outside of the semiconductor chip and may reach the plurality of electrodes that are exposed from the insulating film, making it difficult to connect one end of the plurality of conductive

wires with the plurality of electrodes and possibly causing defective wire bonding. According to the present invention, a groove is formed in the insulating film so as to expose the main surface of the wiring substrate between the plurality of electrodes and the semiconductor chip, preventing the pasty adhesive from flowing beyond the groove to reach the electrodes.

In Toyoshima an edge part of the recess part 13 functions as a dam preventing the outflow of the adhesive 5a. This construction can be used to restrict the flow of adhesive, but it is necessary to secure a sufficient area between the chip and the dam, which is disadvantageous for size reduction.

If the area between the chip and the dam is made too narrow, the adhesive confined in the narrow area, and having nowhere to go, can crawl up onto the top of the dam or onto the main surface of the chip. As a result, a problem can arise, as shown in Fig. 37 of the present application and as described in the present specification at page 8, line 8 to page 9, line 2, namely, in the chip bonding operation adhesive comes into contact with the bonding tool holding the semiconductor chip and contaminates the bonding tool.

In the present invention, however, the groove extending through the insulating film allows the pasty adhesive outflow to stay in the groove, where it does not reach the electrodes or adversely affect the chip bonding operation.

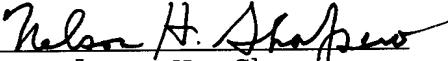
Compare Toyoshima and the present invention as shown in SKETCH 1 and SKETCH 2 submitted herewith.

Accordingly, Claim 31 and the claims dependent thereon and Claim 36 should be allowed.

This application is now believed to be clearly in condition for allowance.

The Commissioner is hereby authorized to charge to Deposit Account No. 50-1165 any fees that may be required by this paper and to credit any overpayment to that Account. If any extension of time is required in connection with the filing of this paper and has not been requested separately, such extension is hereby requested.

Respectfully submitted,

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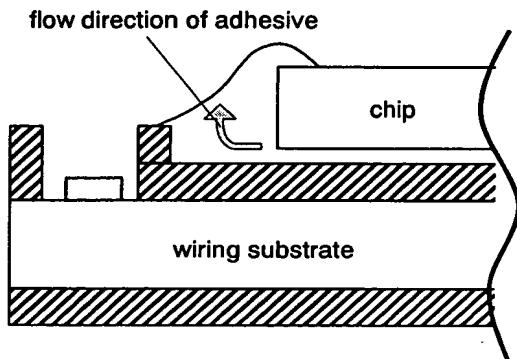
AMENDMENTS TO THE DRAWINGS:

The attached sheets of drawings include changes to Figs. 34, 35, 36 and 37, and replace the corresponding original sheets of the drawings. In Figs. 34, 35, 36 and 37, "Prior Art" has been added. The lead line from "1" in Fig. 34 has been extended.

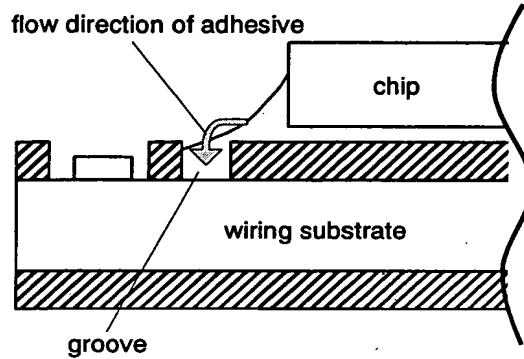
Attachment: Replacement Sheets  
Annotated Sheets Showing Changes



USPA No.: 10/825,678



SKETCH 1. Toyoshima



SKETCH 2. our invention

FIG. 34 PRIOR ART

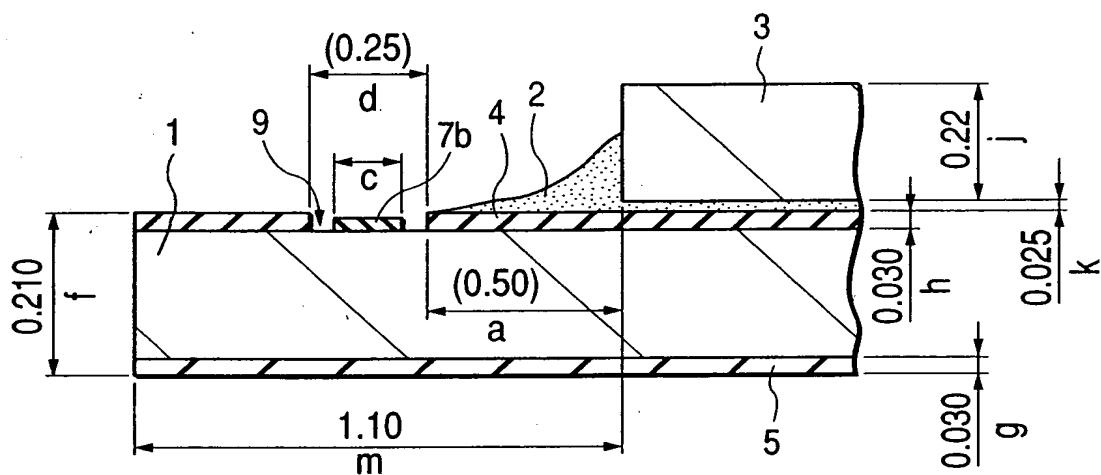
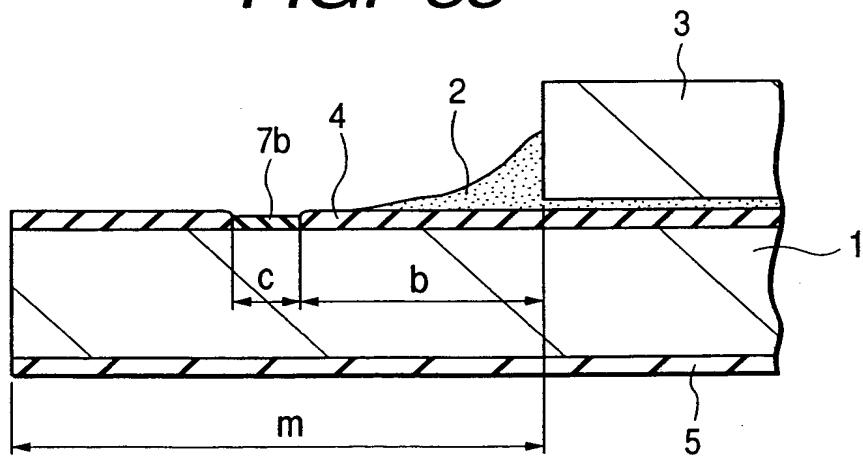
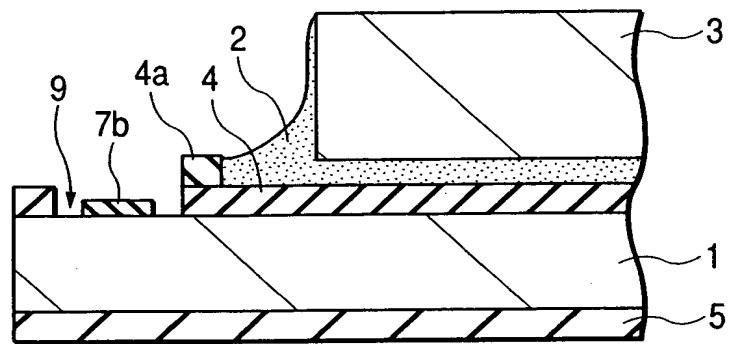


FIG. 35 PRIOR ART



**FIG. 36** PRIOR ART



**FIG. 37** PRIOR ART

